(12) PATENT APPLICATION PUBLICATION
(19) INDIA
(22) Date of filing of Application :27/06/2021

(21) Application No.202141028833 A
(43) Publication Date : 16/07/2021

(54) Title of the invention : OPTIMIZED ULTRALARGE SCALE SOC TEST CONTROL ARCHITECTURE WITH SCAN TEST FOR BANDWIDTH MANAGEMENT

(51) International classification	:G01R0031318500, H01L0027120000, H01S0003160000, G01R0031317700, G11C0029400000
(31) Priority Document No	:NA
(32) Priority Date	:NA
(33) Name of priority country	:NA
(86) International Application No Filing Date	:PCT// :01/01/1900
(87) International Publication No	: NA
(61) Patent of Addition to Application Number Filing Date	:NA :NA
(62) Divisional to Application Number Filing Date	:NA :NA

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(57) Abstract :
This innovation presents various methods for solving issues using scan bandwidth management for big industrial multi-core system-on-chip (SoC) architectures with built-in compression test data. The channel management system, flow, and tools provide critical difficulties in these architectures. Several logic testing designs make it easier to plan preemptive SoC circuits with an integrated deterministic compression of test-based data in this innovation. In actual applications, the same methods may effectively manage physical limitations. Last but not least, state-of-the-art algorithms for SoC test planning are re-designed to establishing timed, efficient test configurations, optimizing SoC pin partitions, and assigning core channel levels based on the volume of scans.

No. of Pages : 22 No. of Claims : 4

Patent Search

Invention Title	OPTIMIZED ULTRALARGE SCALE SOC TEST CONTROL ARCHITECTURE WITH SCAN TEST FOR BANDWIDTH MANAGEMENT
Publication Number	29/2021
Publication Date	16/07/2021
Publication Type	INA
Application Number	202141028833
Application Filing Date	27/06/2021
Priority Number	
Priority Country	
Priority Date	
Field Of Invention	PHYSICS
Classification (IPC)	G01R0031318500, H01L0027120000, H01S0003160000, G01R0031317700, G11C0029400000

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Abstract:

This innovation presents various methods for solving issues using scan bandwidth management for big industrial multi-core system-on-chip (SoC) architectures with built-compression test data. The channel management system, flow, and tools provide critical difficulties in these architectures. Several logic testing designs make it easier to pl preemptive SoC circuits with an integrated deterministic compression of test-based data in this innovation. In actual applications, the same methods may effectively mana physical limitations. Last but not least, state-of-the-art algorithms for SoC test planning are re-designed to establishing timed, efficient test configurations, optimizing SoC p partitions, and assigning core channel levels based on the volume of scans.

Complete Specification

Claims:1) A technique for designing an integrated testing circuit, in which the integrated circuit includes: a variety of built-in I/O pins with a default I/O frequency. Due to a diversity of scanning chains, the integrated circuit being adapted to connect to an integrated circuit control unit through an available number of such a flurry of integrated circuit I/O pins, in the case of the electrical communication with these I/O pins whereby these scan chains predetermine the maximum latching frequency.
(a) Minimizing a testing time for an integrated circuit when the frequency is less than the predetermined maximum I/O frequency. As a result, the number of integrated I pins accessible for the scan design is less than the number of pins needed.
(b) to minimize the said integrated test time when the said assembly frequency is higher than the specified maximum I/O frequency and when the number of pins neede for the proposed scanning architecture is higher than the number of pins available.
2) If the test frequency is lower than that predetermined maximum I/O frequency for that integrated testing unit when the number of built-in testing unit pins is less thar the number of built-in circuit test unit pins and the integrated circuit test frequency is less than that are detected. Then, the pre-detection unit is less than or equal to tha pre-detection.
3) The method according to claim 1, according to which such a step is minimized, includes the use of at least one high-speed Channel for test data in the integral circuit from that integrated circuit control system; the demultiplexing of at least one high-speed Channel on that integrated circuit to a plurality of low-speed channels.
4)The method, according to claim 2, further comprises the steps by which: the collection by the second plurality of slow speed channels of a reply to each of the scan channels at the output and the transmission of answers to the integrated circuit control unit.
Description:The current invention pertains to a Design for solving issues using scan bandwidth management for big industrial multi-core system-on-chip (SoC)

View Application Status